PTO/SB/08B (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet | | of |

Complete if Known	
Application Number	09/994,299
Filing Date	NOVEMBER 26, 2001
First Named Inventor	MIRON ABRAMOVICI
Group Art Unit	2133
Examiner Name	
Attorney Docket Number	487-012

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
DT	1	C. STROUD, S. WIJESURIYA, C. HAMILTON, AND M. ABRAMOVICI, "Built-In Self-Test of FPGA Interconnect," Proc. Intn'l. Test Conf., pp. 404-411, 1998.	
DT	2	I. HARRIS AND R. TESSIER, "Interconnect Testing in Cluster-Based FPGA Architectures", Proc. AMC/IEEE Design Automation Conf., 2000	
DT	3	I. HARRIS AND R. TESSIER, "Diagnosis of Interconnect Faults in Cluster-Based FPGA Architectures", Proc. IEEE Intn'l Conf. on Computer Aided Design, 2000.	
DT	4	M. ABRAMOVICI, ET AL., "Using Roving STARs for On-LineTesting and Diagnosis of FPGAs in Fault-Tolerant Applications," Proc. IEEE Intn'l. Test Conf., pp. 973-982, 1999.	
DT	5	M. ABRAMOVICI, ET AL., "Improving On-Line BIST-Based Diagnosis for Roving STARs," Proc. IEEE Intn'l On-Line Testing Workshop, 2000.	
DT	6	K. ROY AND S. NAG, "On Routability for FPGAs Under Faulty Conditions," IEEE Trans on Computers, Vol. 44, pp. 1296-1305, 1995.	

Examiner Signature		Date Considered	3/4/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

3

COPY OF PAPERS ORIGINALLY FILED

4-4

PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/994,299
Filing Date	NOVEMBER 26, 2001
First Named Inventor	MIRON ABRAMOVICI
Art Unit	2133
Examiner Name	
Attorney Docket Number	487-012

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature	Davidson	Date Considered	3/11/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

4-4

PTO/SB/08B (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet | | of |

Complete if Known	
Application Number	09/994,299
Filing Date	NOVEMBER 26, 2001
First Named Inventor	MIRON ABRAMOVICI
Group Art Unit	2133
Examiner Name	
Attorney Docket Number	487-012

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
DT	1	A. STEININGER AND SCHERRER, "On the Necessity of On-Line BIST in Safety Critical Applications," Proc. 29th Fault-Tolerant Computing Symp", pp. 208-215, 1999.	
DT	2	M. RENOVELL, J. PORTAL, J. FIGUERAS, AND Y. ZORIAN, "Testing the Interconnect of RAM-Based FPGA," Proc. IEEE Design & Test of Computers, Vol. 15, No. 1, pp. 45-50, 1998.	
DT	3	S. DUTT AND F. HANCHECK, "REMOD: A New Methodology for Designing Fault-Tolerant Arithmetic Circuits," IEEE Trans. on VLSI Systems, Vol. 5, pp. 34-56, 1997.	
DT	4	S. DUTT, ET AL., "Efficient Incremental Rerouting for Fault Reconfiguration in Field Programmable Gate Arrays," ACM/IEEE Intn'l Conf. on Computer Aided Design," 1999.	
DT	5	J. EMMERT AND D. BHATIA, "Reconfiguring FPGA Mapped Designs with Applications to Fault Tolerance and Reconfigurable Computing", Lecture Notes on Comp. Sci., Vol. 1304, pp. 141-150, 1997.	
DT	6	J. EMMERT AND D. BHATIA, "A Fault Tolerant Technique for FPGAs", Journal of Electronic Testing, Vol. 16, pp. 591-606, 2000.	
DT	7	F. HANCHEK AND S. DUTT, "Methodologies for Tolerating Logic and Interconnect Faults in FPGAs," IEEE Trans.on Computers, pp. 15-33, 1998.	
DT	8	J. LACH, ET AL., "Low Overhead Fault-Tolerant FPGA Systems," IEEE Trans. on VLSI Systems, Vol. 6, No. 2, pp. 212-221, 1998.	
DT	9	J. LACH, ET AL., "Algorithms for Efficient Runtime Fault Recovery on Diverse FPGA Architectures," Proc. Intn'l. Symp. on Defect and Fault Tolerance In VLSI Systems, 1999.	
DT	10	N. MAHAPATRA AND S. DUTT, "Efficient Network Flow Based Technique for Dynamic Fault Reconfiguration in FPGAs", Proc. Fault Tolerant Computing Symp., pp. 122-129, 1999.	

Examiner Signature	Daniel	Date Considered	3/11/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/994,299
Filing Date	NOVEMBER 26, 2001
First Named Inventor	MIRON ABRAMOVICI
Art Unit	2133
Examiner Name	
Attorney Docket Number	487-012

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature	Dundon	Date Considered	3/11/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

5

PTO/SB/08B (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet | | of | |

Complete if Known	
Application Number	09/994,299
Filing Date	NOVEMBER 26, 2001
First Named Inventor	MIRON ABRAMOVICI
Group Art Unit	2133
Examiner Name	
Attorney Docket Number	487-012

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
DT	1	C. ZENG, N. SAXENA and E. McCLUSKEY, "Finite State Machine Synthesis With Concurrent Error Detection", Proc. IEEE Int'l. Test Conf., 1999, pp. 672-6789.	

Examiner Signature	Davidson	Date Considered	3/11/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

COPY OF PAPE
ORIGINALLY FILED

PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/994,299
Filing Date	NOVEMBER 26, 2001
First Named Inventor	MIRON ABRAMOVICI
Art Unit	2133
Examiner Name	
Attorney Docket Number	487-012

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	3/11/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

6

COPY OF PAPERS
ORIGINALLY FILED

PTO/SB/08B (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet | | of |

Complete if Known	
Application Number	09/994,299
Filing Date	NOVEMBER 26, 2001
First Named Inventor	MIRON ABRAMOVICI
Group Art Unit	2133
Examiner Name	
Attorney Docket Number	487-012

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
DT	1	F. LOMBARDI, D.ASHEN, X. CHEN, and W.K. HUANG, "Diagnosing Programmable Interconnect Systems for FPGAs," Proc. ACM/SIGDA Intn'l. Symp. on FPGAs, pp. 100-106, 1996.	
DT	2	J. EMMERT and D. BHATIA, "Incremental Routing in FPGAs", Proc. IEEE Int'l. ASIC Conf., pp. 302-305, 1998.	

Examiner Signature	Daniel Tran	Date Considered	3/11/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.